EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 5

2/27/24 - 3/5/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

This week, we ran into more issues with integrating the inverter into the Caravel harness. We also started prototyping a comparator for use in our ADC and started looking into the process parameters for this.

Past Week Accomplishments:

- Began inverter integration with Caravel Harness wrapper
- Began formulating prototyping plans for ADC architectures are ADC subsystem

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Spent time debugging caravel harness integration. Looked into setting up ReRAM in the tool flow	7	35
Gage Moorman	Researched and Began testing Comparator architecture	6	34
Nathan Cook	Got some of ReRAM digital design completed	6	33
Jason Xie	Continued debugging caravel harness integration.	6	34

Pending Issues:

- When integrating the inverter with the Caravel Harness, there are a couple of pins that trigger LVS errors
- ReRAM cells in Xschem are not importing correctly

Plans for the coming week:

- Gage Moorman
  - Begin ADC design process with comparator design
  - Begin prototyping ADC design and figuring out best implementation
  - Find process parameters for analog design online or obtain them from simulations
  - Comparator Design
- Konnor Kivimagi
  - Try to simulate a basic ReRAM cell in Xschem to verify that the files are imported correctly.
  - Iron out any final kinks in the analog tool flow
  - Start on documentation
- Nathan Cook
  - Finish ReRAM cell digital, test and verify
  - Write ADC in digital domain
    - If finished early start on DAC
- Jason Xie
  - Debug inverter integration LVS errors
  - Determine comparator design parameters
  - Begin looking into digital representation of ReRAM Crossbar

Summary of Advisor Meeting:

During the advisor meeting, we discussed the resolution of our ADC and the plan to make an 8-bit ADC. After some discussion, we decided on a 3-4-bit ADC as anything bigger would provide no additional benefit. We also addressed our personas and got some more clarification on what type of users would be interested in our design.